D. Remarks

Rejection of Claims 1, 2-3, 6-7, 21-24, and 26-27 Under 35 U.S.C. §102(e) based on *Hung et al.* (USPAP 2002/0132403).

The rejection of claims 1, 2-3, and 6-7 will first be addressed.

The semiconductor device of amended claim 1 includes an insulated gate field effect transistor (IGFET). A gate electrode of the IGFET includes a lower layer electrode formed on a gate insulating film and an upper layer electrode formed on the lower layer electrode. A cap film is formed on the upper layer electrode. A first nitride film is on a side surface of the upper layer electrode. The first nitride film has a film thickness of approximately 2 to 5 nm. The IGFET includes an oxide film on a side surface of the lower electrode and an etching stopper film including a second nitride film formed on the outside of the first nitride film and an outside surface of the oxide film.

As is well known, a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference.

Hung et al. discloses an IGFET having a cap film 8, a metal silicide layer 6a, and a polysilicon layer 6. The IGFET includes a silicon dioxide layer 10, a nitride liner layer 12, and a borderless nitride layer 20 (alleged to correspond to applicants etcher stopper film of amended claim 1).[1] In *Hung et al.*, borderless nitride layer 20 is formed on an outside surface of nitride liner layer 12 and not on an outside surface of the oxide film as recited in amended claim 1.

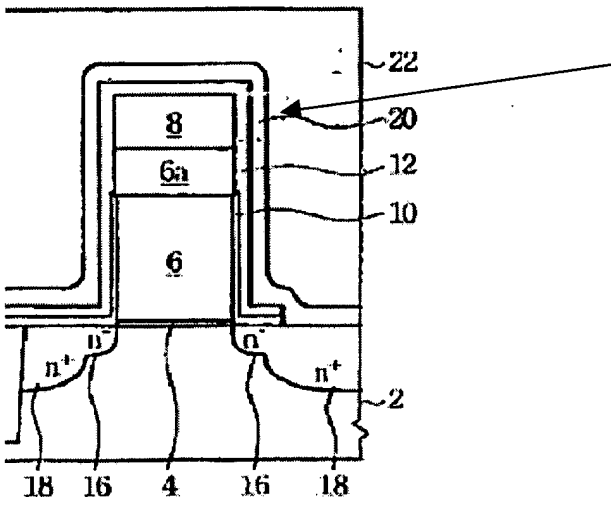

FIG. 5 of *Hung et al.* showing borderless nitride layer formed on an outside surface of nitride liner layer 12 and not on an outside layer of silicon dioxide layer 10.

[1] See page 2, last paragraph of Office Action dated 12/29/04.

Accordingly, because the reference *Hung et al.* does not show all elements of amended claim 1, this ground of rejection is traversed.

The rejection of claims 21-24, 26 and 27 will now be addressed.

The semiconductor device of claim 21 includes a first transistor formed in a first region. The first transistor includes a first upper layer gate electrode formed on and in electrical connection with a first corresponding lower layer gate electrode. A first insulating film formed on a side surface of the first lower layer gate electrode and not on the side surface of the first upper layer gate electrode. A second insulating film formed on a side surface of the first upper layer gate electrode. The second insulating film having a lower thermal growth rate with respect to the first upper layer gate electrode material than the thermal growth rate of the first insulating film with respect to the first lower layer gate electrode material. A first etching stopper is formed on the outside of the first and second insulating films. The second insulating film has a thickness of less than 6 nm.

Hung et al. discloses an IGFET having a cap film 8, a metal silicide layer 6a (alleged to correspond to applicants first upper gate electrode of claim 21)[2], and a polysilicon layer 6. The IGFET includes a silicon dioxide layer 10 (alleged to correspond to applicants first insulating film of claim 21)[3], a nitride liner layer 12, and a borderless nitride layer 20. In *Hung et al.*, silicon dioxide layer 10 is formed on a side surface of polysilicon layer 6 and a side surface of the metal silicide layer 6a.

Hung et al. describes the silicon dioxide layer 10 as being optionally formed on the surface of the gate and substrate by thermal process.[4] However, *Hung et al.* makes no mention of excluding the formation of the silicon dioxide layer 10 on the side surface of the metal silicide layer 6a nor does *Hung et al.* disclose any mechanism of excluding the growth of the silicon dioxide layer from growing on the metal silicide layer 6a. In *Hung et al.*, silicon dioxide layer 10 is formed immediately after an etching step forms the stacked gate structure.[5] At this time, the side surface of metal silicide 6a would be exposed to the oxidation step.

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[2] See page 3, 3rd paragraph of Office Action dated 12/29/04
[3] See page 3, 3rd paragraph of Office Action dated 12/29/04
[4] See *Hung et al.*, first sentence of paragraph 0020.
[5] See *Hung et al.* paragraph 0019 to first sentence of paragraph 0020.

It is noted in applicant's background that a silicide material may be more likely to oxidize than polysilicon.[6]

Furthermore, Figure 5 of *Hung et al.* shows the silicon dioxide layer 10 at least covering the bottom of the side surface of silicide layer 6a.

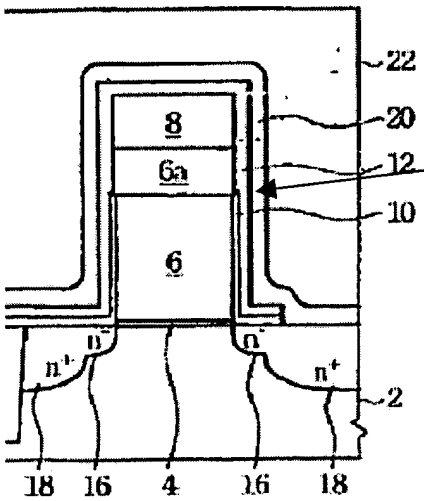

FIG. 5 of *Hung et al.* showing silicon dioxide layer 10 at least covering the bottom of the side surface of silicide layer 6a.

Because the reference *Hung et al.* does not show all elements of claim 21, this ground of rejection is also traversed.

Rejection of Claims 2-3, 6-7, 21-24, 26-27 Under 35 U.S.C. §103(a), based on *Hung et al.*

As is well known, in proceedings before the Patent and Trademark Office, the examiner bears the burden of establishing a prima facie case of obviousness based on the prior art.[7] In addition, to establish a prima facie case of obviousness, a rejection must meet three basic criteria. First, there must be some suggestion or motivation to modify a reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference(s) must teach or suggest all claim limitations.[8]

To address the rejection of claims 2-3 and 6-7, the arguments set forth above with regard to the rejection of amended claim 1 are incorporated herein by reference. Namely, *Hung et al.* does not teach or suggest an etching stopper film including a second nitride film formed on the outside of the first nitride film and an outside surface of the oxide film.

Because *Hung et al.* does not teach or suggest all the limitations of amended claim 1 upon

[6] See page 4, lines 15-16 of the Specification.
[7] Ex parte Obukowicz, 27 USPQ 1063, 105 (B.P.A.I. 1992).
[8] MPEP §2143.

which claims 2-3 and 6-7 are based, this ground of rejection is traversed.

To address the rejection of claims 21-24, 26, and 27, the arguments set forth above with respect to claim 21 are incorporated herein by reference. Namely, because *Hung et al.* does not teach or suggest a first insulating film formed on a side surface of the first lower layer gate electrode and not on the side surface of the first upper layer gate electrode as required in claim 21, this ground of rejection is traversed.

Rejection of Claims 5 and 25 Under 35 U.S.C. §103(a), based on *Hung et al.* in view of *Liaw* (USP 6,448,140).

The invention of claim 5 includes an interlayer insulating film formed to cover the gate electrode of the IGFET, a contact hole opened in the interlayer insulating film to expose a source/drain region of the IGFET, and a conductor filling the contact hole and electrically connected with the source/drain region.

To address this rejection, to the extent relied on by *Hung et al.*, the arguments set forth above with respect to claim 1 are incorporated herein by reference. Namely, *Hung et al.* does not teach or suggest an etching stopper film including a second nitride film formed on the outside of the first nitride film and an outside surface of the oxide film.

Liaw also does not teach or suggest the etching stopper film as required in amended claim 1. In figure 5, *Liaw* shows silicon nitride spacers 10. However, these silicon nitride spacers are not formed on the outside of a first nitride film as recited in amended claim 1, from which claim 5 depends.

Further, as is also well established, a prima facie case of obviousness may be rebutted by showing that the art, in any material respect, teaches away from the claimed invention.[9]

Liaw teaches away from applicant's invention. More specifically, *Liaw* teaches away from a first nitride film on a side surface of the upper layer electrode as recited in amended claim 1. *Liaw*'s purpose is to form a straight walled polycide gate structure.[10] *Liaw* accomplishes this by creating a lateral recess of a tungsten silicide layer 8.[11] Then a silicon oxide sidewall layer 9b and 9c is thermally grown on exposed sidewalls of polysilicon 3 and tungsten silicide 8. Due to the different growth rates, a 100 to 400 Angstrom silicon oxide layer is grown on the tungsten

[9] In re Geisler, 43 USPQ2d 1362, 1366 (Fed. Cir. 1997).
[10] See *Liaw* column 2, lines 19-21.
[11] See *Liaw,* Fig. 3 in conjunction with column 4, lines 55-65.

silicide sidewall and a 50 to 200 Angstrom silicon oxide layer is grown on the polysilicon sidewall. In this way, a silicon oxide layer having a straight sidewall is formed.[12]

Liaw teaches away from Applicant's claim limitations, as a first nitride film would inhibit the growth of silicon oxide on the tungsten silicide layer 8 as compared to the polysilicon 3. *Liaw* relies on silicon oxide formed on the tungsten silicide layer 8 having a higher growth rate.

Accordingly, because *Liaw* teaches away from the claimed invention, any prima facie case has been rebutted.

The rejection of claim 25 will now be addressed.

Claim 25 depends from claim 21 and recites that the first lower layer gate electrode has a greater length than the first upper layer gate electrode.

To address this rejection, to the extent the rejection relies on *Hung et al.*, the arguments set forth above with respect to claim 21 are incorporated herein by reference. Namely, *Hung et al.* does not teach or suggest a first insulating film formed on a side surface of the first lower layer gate electrode and not on the side surface of the first upper gate electrode.

Liaw also does not teach or suggest the first insulating film of claim 21. *Liaw* shows the same layer (silicon oxide layer 9b and 9c) on the side surface of polysilicon layer 3 and tungsten silicide layer 4.

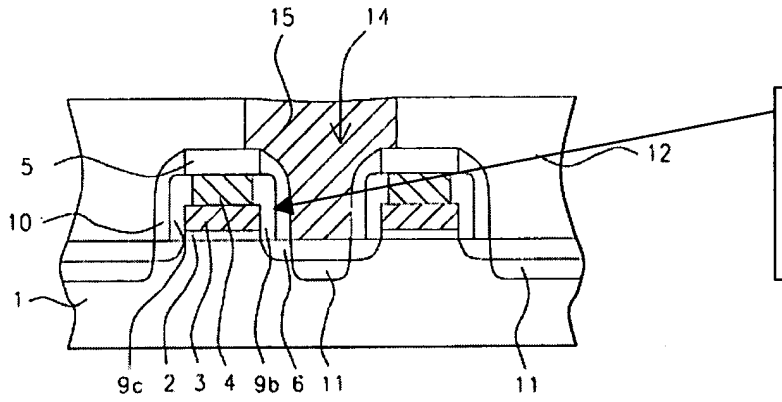

FIG. 7 of *Liaw* showing the same silicon oxide layer (9b and 9c) formed on the side surface of polysilicon layer 3 and tungsten silicide layer 4.

Furthermore, *Liaw* teaches away from the invention of claim 21 from which claim 25 depends. Claim 21 includes a second insulating film formed on a side surface of the first upper layer gate electrode. The second insulating film has a lower thermal growth rate with respect to the first upper layer gate electrode material than the thermal growth rate of the first insulating

[12] *See Liaw, FIG. 4 in conjunction with column 5, lines 4-28.*

film with respect to the first lower layer gate electrode. As noted in the arguments set forth above with respect to claim 5, *Liaw* relies on the silicon oxide 9c formed on the tungsten silicide layer 3 having a higher growth rate of the silicon oxide 9b formed on the polysilicon layer 3. In this way, the purpose of *Liaw* (having stacked gate structure having a straight sidewall structure) is obtained.[13]

For all of these reasons, this ground of rejection is traversed.

Claim 1 has been amended. New claim 29 has been added. Claim 29 includes features of allowed claim 17 and thus cannot necessitate a new search.

The present claims 1-3, 5-7 and 17-29 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

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[13] See *Liaw* column 5, lines 4 to 27.